Shenzhen Leadtek Electronics Co.,Ltd

PRODUCT SPECIFICATION

TFT-LCD MODULE

Module No：LTK034MNBCT12-V0

☑ Preliminary Specification

☐ Approval Specification

Designed by	Checked by	Approved by
jona	Jerry	lan

Final Approval by Customer

Approved by	Comment

※The specification of “TBD” should refer to the measured value of sample . If there is difference between the design specification and measured value, we naturally shall negotiate and agree to solution with customer.

1.Document Revision History

Version	**Contents**	**Date**	**Note**
V0	**NEW**	**2023.12.07**	

2. General Description

N0	Item	Specification	Unit	Remark
1	LCD Size	TFT"3.4	inch	-
2	Panel Type	IPS	-	-
4	Number of pixels	800 x RGB x 800	pixel	-
5	Display mode	Normally Black	-	-
6	Display colors	16.7M	-	-
7	Viewing Direction	ALL	-	-
8	Contrast Ratio	1200	-	
9	Luminance	300	nit	
10	CTP+LCM Module Size	109.20 (W) x113.47(L) x3.77(T)	mm	Note
11	Active Area	87.60 (W) x 87.60 (L)	mm	Note
12	Pixel Pitch	0.0365 (H) × 0.1095 (V)	mm	-
13	Weight	TBD	g	-
14	Driver IC	FL7705NI-G	bit	-
15	Light Source	8 white LED	-	-
16	Interface	MIPI	-	-
17	Operating Temperature	-20~+70	℃	-
18	Storage Temperature	-30~+80	℃	-

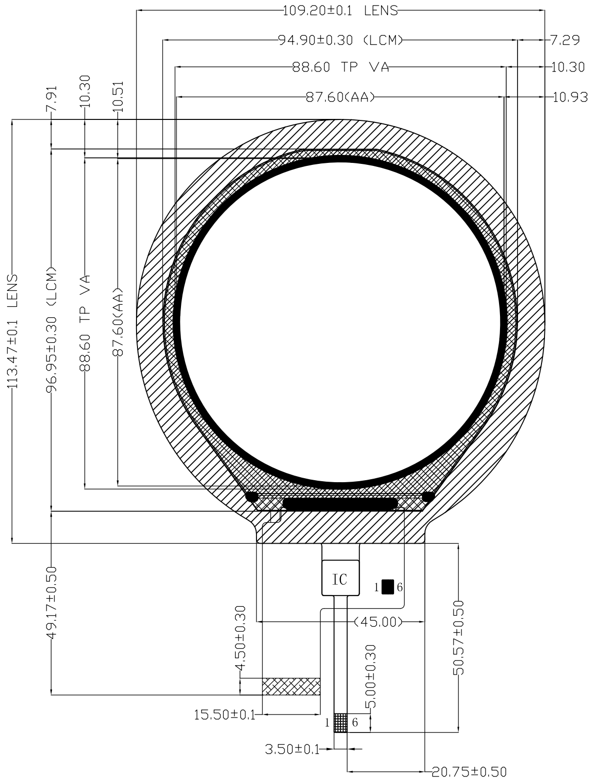
3. 0 Pin Assignment

3.1 LCD Pin assignment

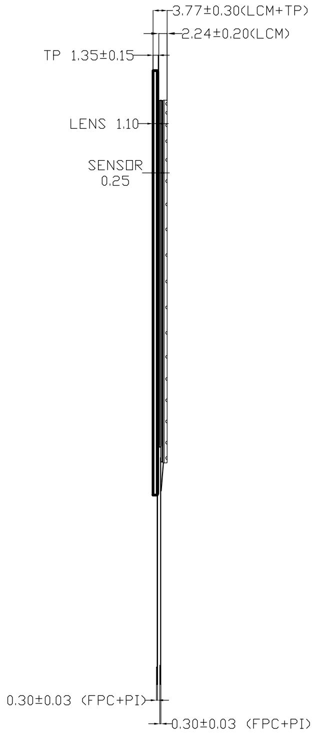
N	Symbol	I/O	Description	Remark
1	LEDA	p	LED Anode	
2	LEDA	p	LED Anode	
3	LEDK	p	LED Cathode	
4	LEDK	P	LED Cathode	
5	VCI	P	Power Supply 2.8V	
6	IOVCC	I	LCD I/O power supply(1.8V)	
7	RESET	-	Reset pin	
8	NC	-	No connection.	
9	GND	P	Ground	
10	D0P	I/O	MIPI DSI differential data pair (Data lane 0)	
11	D0N	I/O	MIPI DSI differential data pair (Data lane 0)	
12	GND	P	Ground	
13	D1P	I	MIPI DSI differential data pair (Data lane 1)	
14	D1N	I	MIPI DSI differential data pair (Data lane 1)	
15	GND	P	Ground	
16	CLKP	I	MIPI DSI differential clock pair	
17	CLKN	I	MIPI DSI differential clock pair	
18	GND	P	Ground	
19	D2P	I	MIPI DSI differential data pair (Data lane 2)	
20	D2N	I	MIPI DSI differential data pair (Data lane 2)	
21	GND	P	Ground	
22	D3P	I	MIPI DSI differential data pair (Data lane 3)	
23	D3N	I	MIPI DSI differential data pair (Data lane 3)	
24	GND	P	Ground	
25	TP-GND	-	Touch Ground	
26	TP_INT	-	Touch Interrupt,No connection	
27	TP_SDA	-	Touch IIC Data signal,No connection	
28	TP_SCL	-	Touch IIC Clock signal,No connection	
29	TP_RESET	-	Touch Reset Signal,No connection	
30	TP_VCI	-	Touch Power supply,No connection	

4 .EXTERNAL DIMENSIONS

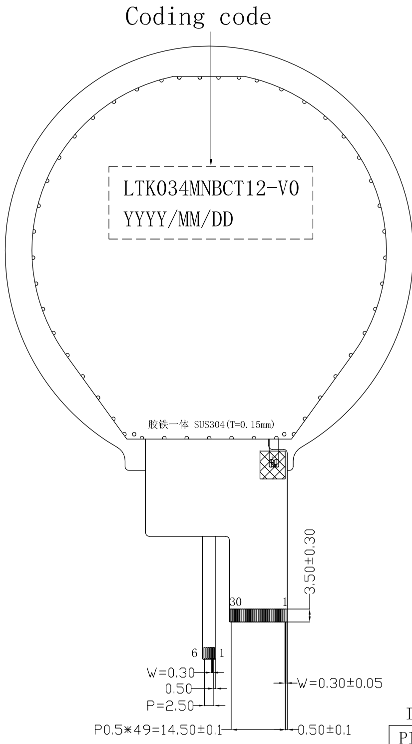
Front View



Side View



Back View



PIN	SYMBOL
1	LEDA
2	LEDA
3	LEDK
4	LEDK
5	VCI
6	IOVCC
7	RESET
8	NC
9	GND
10	D0P
11	D0N
12	GND
13	D1P
14	D1N
15	GND
16	GLKP
17	GLKN
18	GND
19	D2P
20	D2N
21	GND
22	D3P
23	D3N
24	GND
25	TP_GND
26	TP_INT
27	TP_SDA
28	TP_SCL
29	TP_RESET
30	TP_VCI

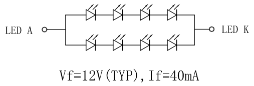
IC: CST836U

PIN	DEFINE
1	GND
2	TP-INT
3	TP-SDA
4	TP-SCL
5	TP-RESET
6	TP-VCI

Technical parameters:
GF
ITO GLASS: 0.25 mm
GLASS LENS: 1.1 mm
IC: CST836U

1. Operating voltage :2.8V-3.3V
2. Transmittance :≥ 85%
3. Surface hardness: ≥6H
4. Working environment: -20℃~+60℃, ≤85%RH
5. Storage environment: -30℃ to +70℃, ≤85%RH
6. The unmarked dimension tolerance is ±0.2mm

Notes:
1. Display: 3.4″,TFT
2. Resolution: 800*RGB*800
3. LCD Viewing Direction: ALL
4. LCD Driver:FL7705NI-G
5. LCM+TP Brightness:300cd/m²(TYP),Uniformity≥80%
6. *:Critical dimension:( )Reference dimension
7. Operating Temperature:-20℃~ +70℃
8. Storage Temperature:-30℃~ +80℃
9. Requirements on Environmental Protection: ROHS



Vf=12V(TYP),If=40mA

REV	DESCRIPTION	DATE	NAME
3			
2			
1			
0	NEW	2023.10.16	JACK

LEADTEK DISPLAY

LEADTEK COMPANY LIMITED

SCALE:1/1	UNIT:mm	PAGE:1/1		Approve	Check	Drawn
Part No:	LTK034MNBCT12	VER:V0		IAN	JONA	JACK
Customer No:						

5. Absolute Maximum Ratings

Ta = 25℃

Item	Symbol	Min.	Max.	Unit	Remark
Power Voltage	VCI	-0.30	+5.6	V	
	IOVCC	-0.30	+4.5	V	
	TP_VCI	3.3	-	V	
	TP_IOVCC	-	-	V	
Operating Temperature	Top	-20	70	℃	
Storage Temperature	T_{st}	-30	80	℃	
Operating and Storage Humidity	H_{stg}	10%	90%	%(RH)	

6. Electrical Characteristics

6.1 Recommended Operating Condition

VCI=3.3V，GND=0V，Ta = 25℃

Item		Symbol	Min.	Typ.	Max.	Unit	Remark
Digital supply Voltage		IOVCC	1.65	1.8	3.3	V	
Analog supply Voltage		VCI	2.8	3.0	3.3	V	
TP Power		TP_VCI	-	3.0	3.3	V	
Input Signal Voltage	Low Level	V_{IL}	0	-	0.3 x IOVCC	V	
	High Level	V_{IH}	0.7 x IOVCC	-	IOVCC	V	
Current of digital supply voltage		I_{IOVCC}	-	16	30	mA	VCI=3.3V, color bar pattern
Current of analog supply voltage		I_{VCI}	-	27	50	mA	

6.2 Backlight Unit Driving Condition

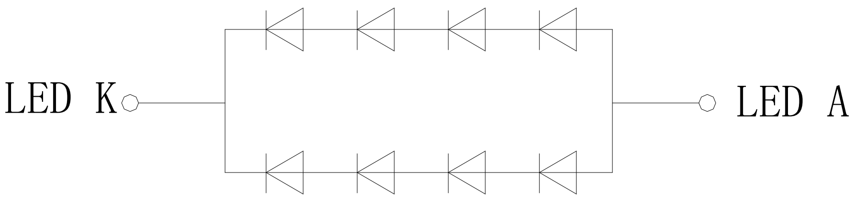
Item	Symbol	Min.	Typ.	Max.	Unit	Remark
Forward Current	I_F	-	40	--	mA	8LEDs (4 LED Serial, 2LED Parallel)
Forward Current Voltage	V_F	-	12.0	--	V	
Backlight Power Consumption	W_{BL}	-	480	--	mW	
Operating Life Time	--	20000	--	--	hrs	Note 2, Note 3

Note1: The LED driving condition is defined for each module (4 LED Serial, 2 LED Parallel).

Note2: When LCM is operated, the stable forward current should be inputted. And forward voltage is for reference only.

Note3: Optical performance should be evaluated at Ta=25℃ When LED is driven at high current, high ambient temperature & humidity condition. The life time of LED will be reduced. Operating life means brightness goes down to 50% initial brightness. Typical operating life time is estimated data.

Note4: The LED driving condition is defined for each LED module.



7. Timing Chart

7.1 DSI Interface Timing Characteristics

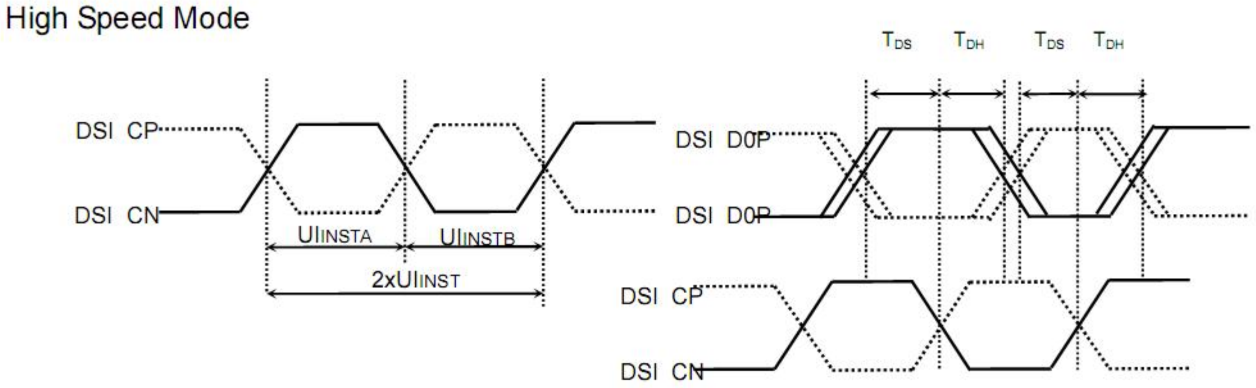


Figure 7.4: DSI clock timing Characteristics

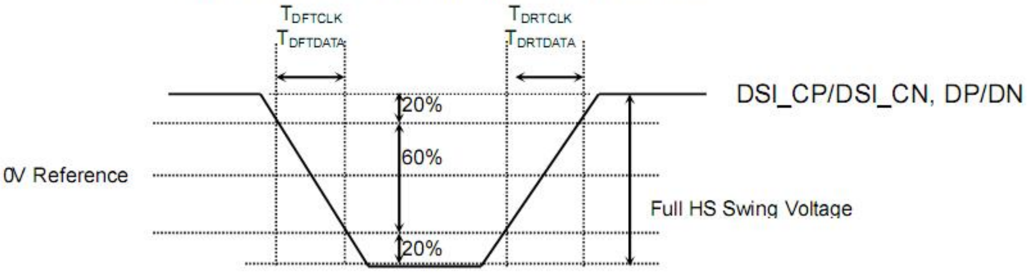


Figure: Rising and falling time on clock and data channel

(VSSA=0V, IOVCC=1.65V to 3.3V, VCI=2.5V to 3.3V, T_A = -30 to 70°C)

Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_CP/ DSI_CN	Double UI instantaneous	$2xU_{INST}$	TBD	-	25	ns
	UI instantaneous	U_{INSTA} U_{INSTB}	TBD	-	12.5	ns
DP/DN	Data to clock setup time	T_{DS}	0.15xUI	-	-	ps
	Data to clock hold time	T_{DH}	0.15xUI	-	-	ps
DSI_CP/ DSI_CN	Differential rise time for clock	T_{DRTCLK}	150	-	0.3UI	ps
	Differential fall time for clock	T_{DFTCLK}	150	-	0.3UI	ps
DP/DN	Differential rise time for data	$T_{DRTDATA}$	150	-	0.3UI	ps
	Differential fall time for data	$T_{DFTDATA}$	150	-	0.3UI	ps

Table: DSI High Speed Mode characteristics

Low Power Mode

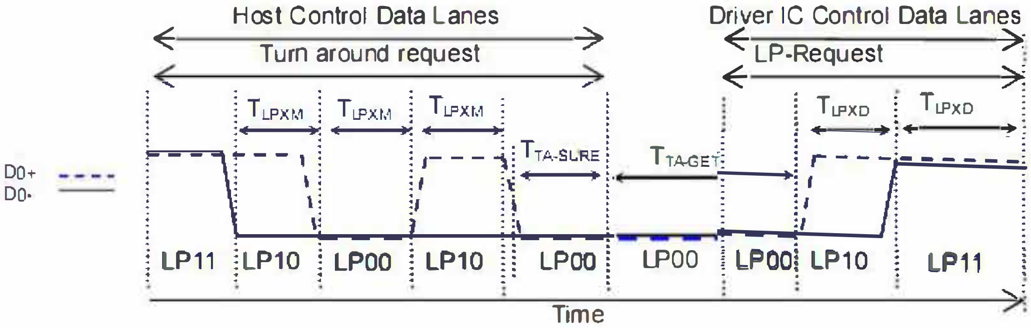


Figure 7.6: BTA from HOST to Display module Timing

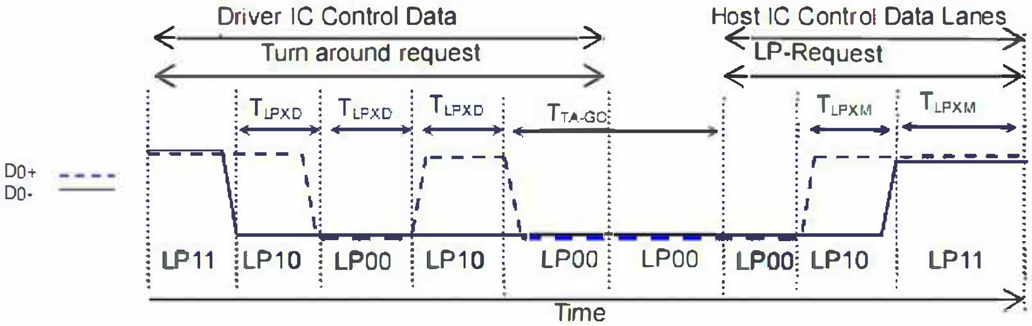


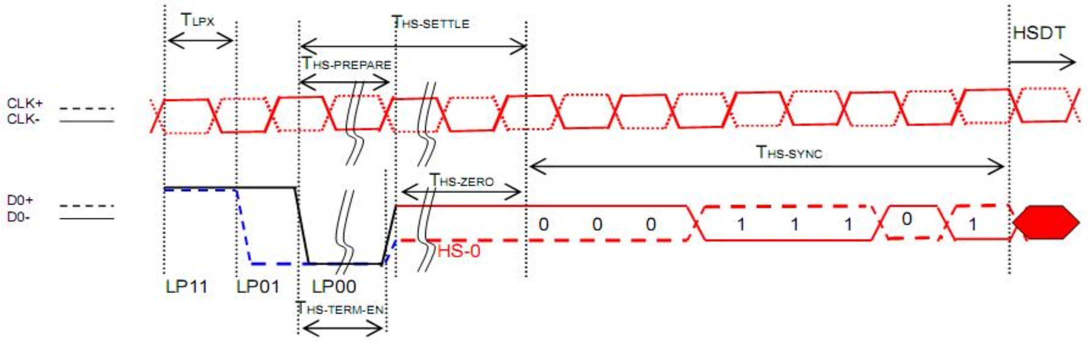
Figure: BTA from Display module Timing to HOST

(VSSA=0V, IOVCC=1.65V to 3.3V, VCI=2.3V to 3.3V,T_A = -30 to 70°C)

Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_D0P/ DSI_D0P	Length of LP-00/LP01/LP10/LP11 Host→ Display module	T_{LPXM}	50	-	-	ns
	Length of LP-00/LP01/LP10/LP11 Display module →Host	T_{LPXD}	50	-	-	ns
	Time-out before the MPU start driver	$T_{TA-SURE}$	T_{LPXD}	-	2xT_{LPXD}	ns
	Time to drive LP-00 by display module	T_{TA-GET}	5xT_{LPXD}	-	-	ns
	Time to drive LP-00 after turnaround request Host	T_{TAGO}	4xT_{LPXD}	-	-	ns

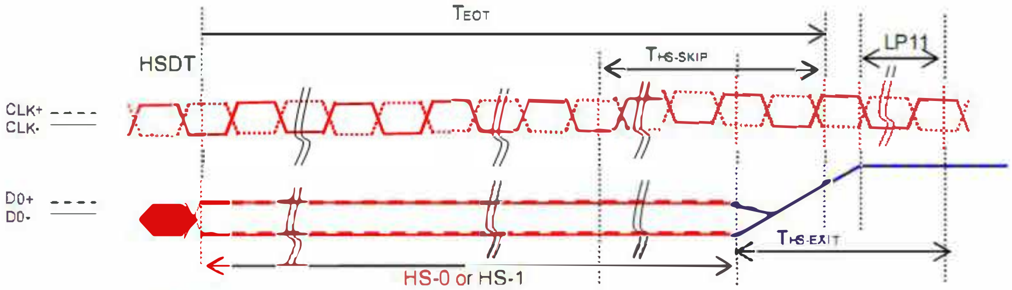
Table: DSI Low Power Mode characteristics

DSI BURSTS



Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_D0P/ DSI_D0P	Length of LP-00/LP01/LP10/LP11	T_{LPX}	50	-	-	ns
	Time to Driver LP-00 to prepare for HS transmission	$T_{HS-PREPARE}$	40+4UI	-	85+6UI	ns
	Time to enable data receiver line termination	$T_{HS-TERM-EN}$	-	-	35+4xUI	ns
	Time to drive LP-00 by display module	T_{TA-GET}	5xT_{LPXD}	-	-	ns
	Time to drive LP-00 after turnaround request Host	T_{TAGO}	4xT_{LPXD}	-	-	ns

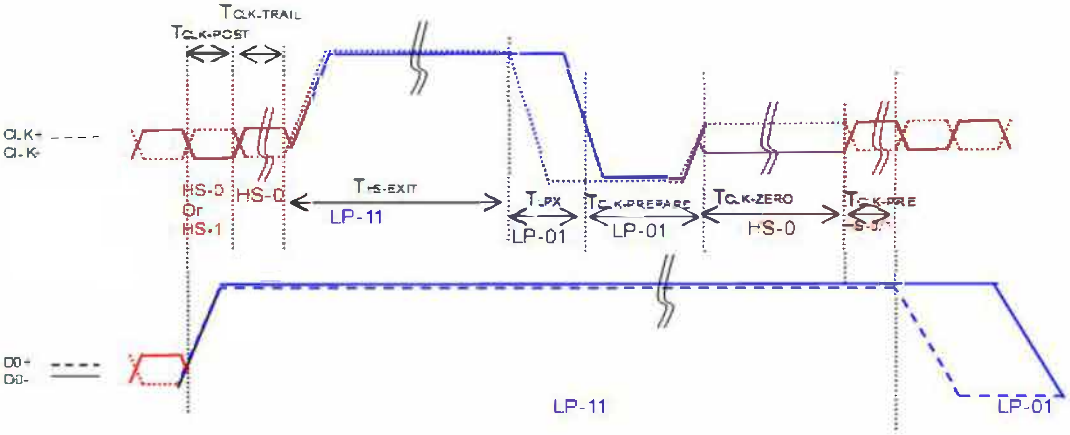
Table: DSI Low Power Mode to High Speed Mode Timing



NOTE:
If the last bit is HS-0, the transmitter changes from HS-0 to HS-1
If the last bit is HS-0, the transmitter changes from HS-1 to HS-0

Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_D0P/ DSI_D0P	Time-Out at Display Module to Ignore Transition Period of EoT	THS-SKIP	40	-	55+4xUI	ns
	Time to Driver LP-11 after HS Burst	THS-EXIT	100	-	-	ns

Table: DSI Low Power Mode to High Speed Mode Timing



Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_CP/ DSI_CN	Time that the MCU shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode	TCLK-POST	60+52xUI	-	-	ns
	Time to drive HS differential state after last payload clock bit of a HS transmission burst	TCLK-TRAIL	60	-	-	ns
	Time to drive LP-11 after HS burst	THS-EXIT	100	-	-	ns
	Time to drive LP-00 to prepare for HS transmission	TCLK-PREPARE	38	-	95	ns
	Time-out at Clock Lane Display Module to enable HS Termination	TCLK-TERM-EN	-	-	38	ns
	Minimum lead HS-0 drive period before starting Clock	TCLK-PREPARE + TCLK-ZERO	300	-	-	ns
	Time that the HS clock shall be driven prior to any associated data Lane beginning the transition from LP to HS mode	TCLK-PRE	8xUI			

Table: Clock Lanes High Speed Mode to/from Low Power Mode Timings

7.2 Recommended Timing Setting

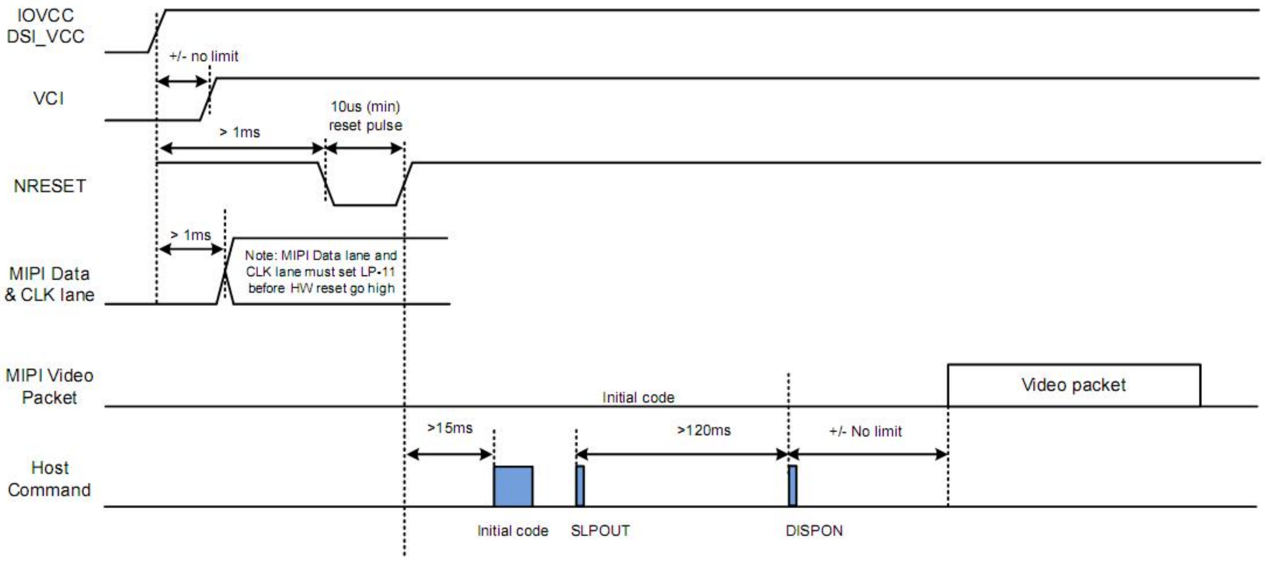
Embedded in Source IC Input Timing (DCLK, HS, VS, DE)

VCI=3.3V, GND=0V, Ta=25℃

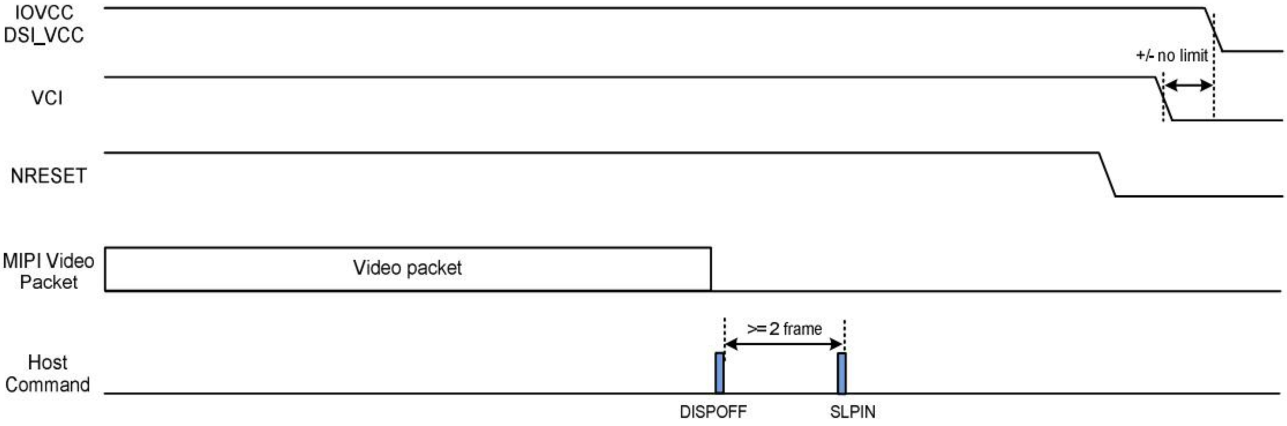
Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
DCLK	Fclk	-	48	-	MHz	
	tclk	-	20.8	-	ns	
HSD	thd	-	800	-	tclk	
	thpw	-	30	-	tclk	
	thb	-	60	-	tclk	
	thfp	-	60	-	tclk	
VSD	tvd	-	800	-	th	
	tvpw	-	4	-	th	
	tvb	-	11	-	th	
	tvfp	-	16	-	th	

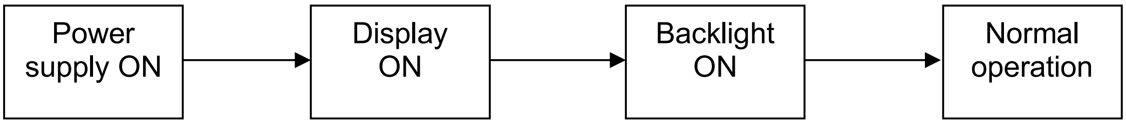
Note: For reference only, it needs to be adjusted according to the actual display effect.

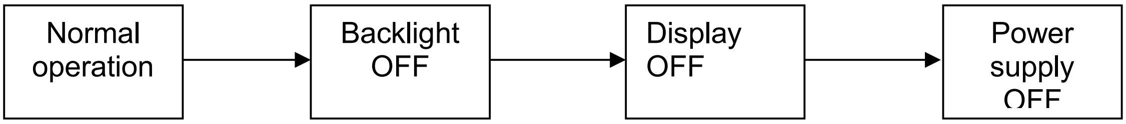
7.3 POWER ON SEQUENCE :



7.4 POWER OFF SEQUENCE :







5.5 Reset timing

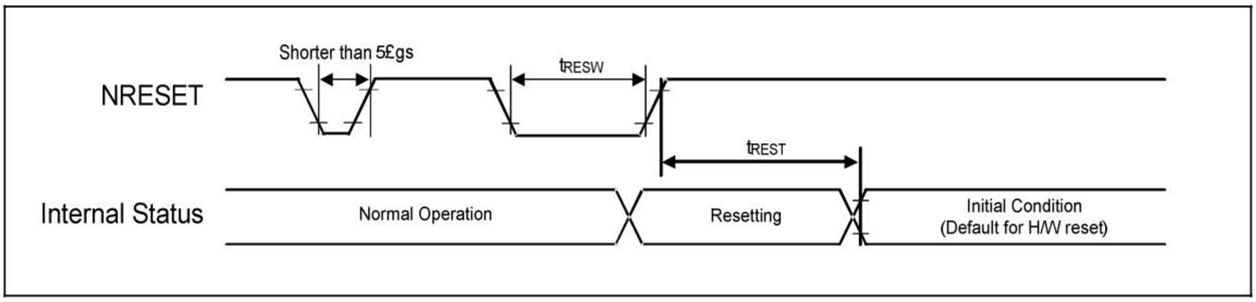


Figure: Reset input timing

Symbol	Parameter	Related Pins	Spec.			Note	Unit
			Min.	Typ.	Max.		
tRESW	Reset low pulse width[1]	NRESET	10	-	-	-	μs
tREST	Reset complete time[2]	-	5	-	-	When reset applied during SLPIN mode	ms
		-	120	-	-	When reset applied during SLPOUT mode	ms

Table: Reset input timing

8. Optical Characteristics

Ta=25℃

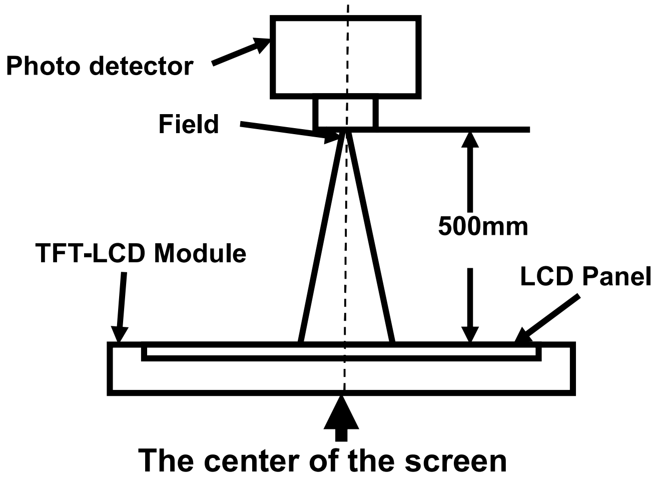
Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
View Angles		θT	CR≧10	80	85	-	Degree	Note 2
		θB		80	85	-		
		θL		80	85	-		
		θR		80	85	-		
Contrast Ratio		CR	θ=0°	1000	1200	-		Note1 Note3
Response Time		T_{ON}	25℃	-	30	35	ms	Note1 Note4
		T_{OFF}						
Chromaticity	White	x	Backlight is on	0.262	0.292	0.322		Note1 Note5
		y		0.303	0.333	0.363		
	Red	x		0.637	0.667	0.697		
		y		0.293	0.323	0.353		
	Green	x		0.241	0.271	0.301		
		y		0.561	0.591	0.621		
	Blue	x		0.104	0.134	0.164		
		y		0.091	0.121	0.151		
Uniformity		U		75	80	-	%	Note1 Note6
NTSC				65	70	-	%	Note 5
Luminance		L		-	300	-	cd/m^2	Note1 Note7

Test Conditions:

1. I_F= 40 mA, V_F=12.8V and the ambient temperature is 25±2℃.humidity is 65±7%
2. The test systems refer to Note 1 and Note 2.

Note 1: Definition of optical measurement system.

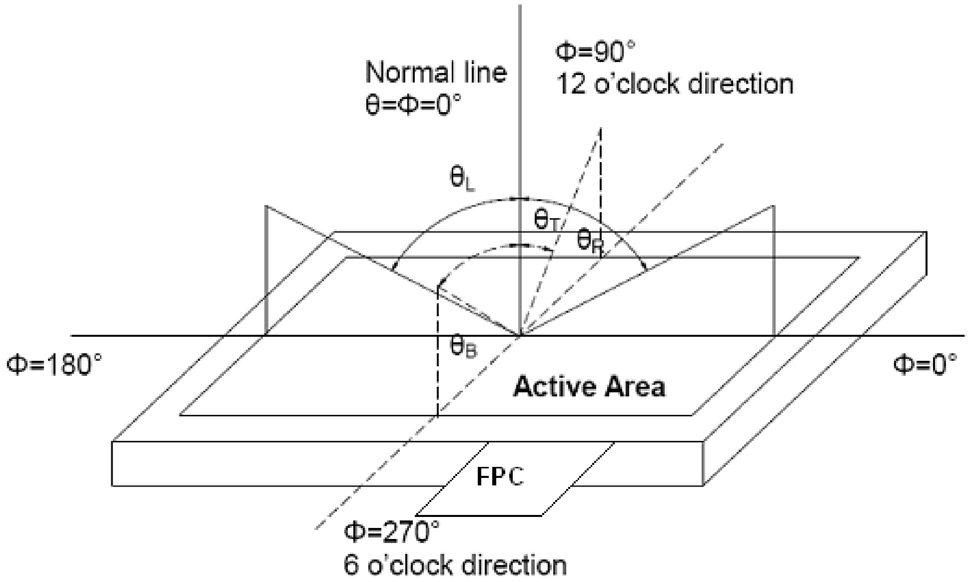
Properties are measured at the center point of the LCD screen. All input terminals LCD panel must be ground when measuring the center area of the panel.



Item	Photo detector	Field
Contrast Ratio	SR-3A	1°
Luminance		
Chromaticity		
Lum Uniformity		
Response Time	BM-7A	2°

Note 2: Definition of viewing angle range and measurement system.

Viewing angle is measured at the center point of the LCD by CONOSCOPE(ergo-80)。



Note 3: Definition of contrast ratio

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD on the "White" state}}{\text{Luminance measured when LCD on the "Black" state}}$$

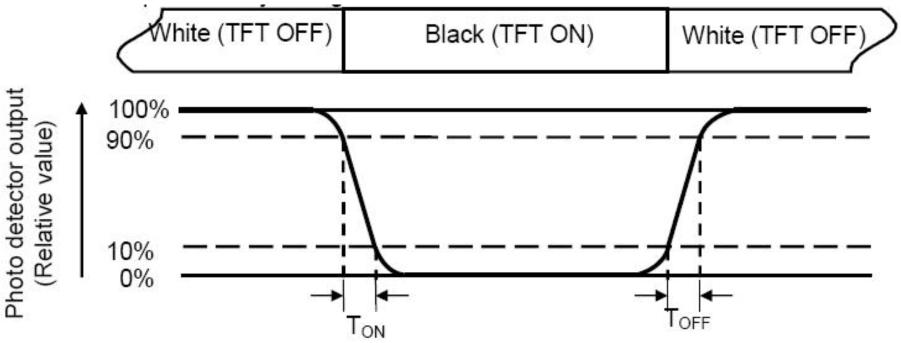
“White state “: The state is that the LCD should drive by Vwhite.

“Black state”: The state is that the LCD should drive by Vblack.

Vwhite: To be determined   Vblack: To be determined.

Note 4: Definition of response time

The response time is defined as the LCD optical switching time interval between “White” state and “Black” state. Rise time (T_{ON}) is the time between photo detector output intensity changed from 90% to 10%. And fall time (T_{OFF}) is the time between photo detector output intensity changed from 10% to 90%.



Note 5: Definition of color chromaticity (CIE1931)

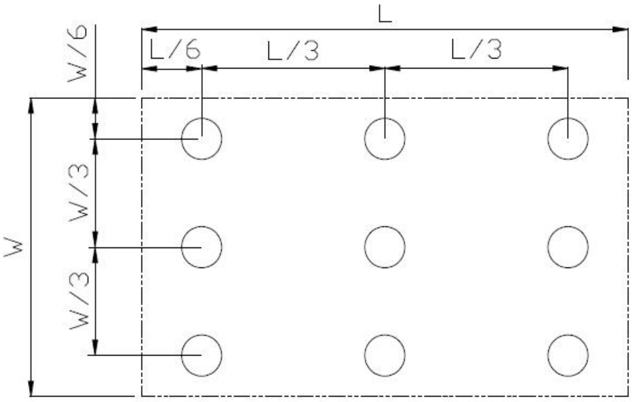
Color coordinates measured at center point of LCD.

Note 6: Definition of luminance uniformity

Active area is divided into 9 measuring areas (Refer Fig. 2). Every measuring point is placed at the center of each measuring area.

Luminance Uniformity (U) = Lmin/ Lmax

L-------Active area length W----- Active area width



Lmax: The measured Maximum luminance of all measurement position.

Lmin: The measured Minimum luminance of all measurement position.

Note 7:Definition of luminance:

Measure the luminance of white state at center point.

9.Environmental / Reliability Test

No	Test Item	Condition	Remarks
1	High Temperature Operation	Ts = +70℃, 240 hours	No abnormalities in functions
2	Low Temperature Operation	Ta = -20℃, 240 hours	No abnormalities in functions
3	High Temperature Storage	Ta = +80℃, 240 hours	No abnormalities in functions
4	Low Temperature Storage	Ta = -30℃, 240 hours	No abnormalities in functions
5	Storage at High Temperature and Humidity	Ta = +60℃, 90% RH max,240hours	No abnormalities in functions
6	Thermal Shock (non-operating)	-30℃ 30 min~ +70℃ 30 min, Change time: 0.5 hour □ 5 min □ 0.5 hour.10 Cycle	Start with cold temperature, End with high temperature,
7	ESD	C=150pF, R=330Ω,5point/panel Air: ±8Kv, 5times; Contact:±4Kv,5times (Environment:15℃~35℃, 30%~60%.86Kpa~106Kpa)	No abnormalities in functions

Note1: Ts is the temperature of panel's surface.

Note2: Ta is the ambient temperature of samples.

10. Precautions for Use of LCD Modules

Handling Precautions

10.1.1 The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.

10.1.2 If the display panel is damaged and the liquid crystal substance inside it leaks out, be sure not to get any in your mouth, if the substance comes into contact with your skin or clothes, promptly wash it off using soap and water.

10.1.3 Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.

10.1.4 The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarizer carefully.

10.1.5 If the display surface is contaminated, breathe on the surface and gently wipe it with a soft dry cloth. If still not completely clear, moisten cloth with one of the following solvents:

— Isopropyl alcohol

— Ethyl alcohol

Solvents other than those mentioned above may damage the polarizer. Especially, do not use the following:

— Water

— Ketone

— Aromatic solvents

10.1.6 Do not attempt to disassemble the LCD Module.

10.1.7 If the logic circuit power is off, do not apply the input signals.

10.1.8 To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.

10.1.8.1 Be sure to ground the body when handling the LCD Modules.

10.1.8.2 Tools required for assembly, such as soldering irons, must be properly ground.

10.1.8.3 To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.

9.1.8.4 The LCD Module is coated with a film to protect the display surface. Be care when peeling off this protective film since static electricity may be generated.

Storage Precautions

10.2.1 When storing the LCD modules, avoid exposure to direct sunlight or to the light of fluorescent lamps.

10.2.2 The LCD modules should be stored under the storage temperature range. If the LCD modules will be stored for a long time, the recommend condition is: Temperature : 0℃ ～ 40℃ Relatively humidity: ≤80%

10.2.3 The LCD modules should be stored in the room without acid, alkali and harmful gas.

Transportation Precautions

10.3.1 The LCD modules should be no falling and violent shocking during transportation, and also should avoid excessive press, water, damp and sunshine.

深圳市丽台电子有限公司

Shenzhen Leadtek Electronics Co.,Ltd

Quality inspection standards

品质允收标准

MODEL No. / 产品型号: Applies 0.95~5.0 TFT-LCD Panel
UPDATED DATE / 生效日期: 2022-05-20
VERSION / 版 本: A0
Customer Signature/客户签字: ____________

RECORD OF REVISION/修订履历：

Version 版本	Revision Record 修订内容	Compile 修订者	Date of Revision 修订日期
V0	首发/Starting	Green	2022.05.20

1.Scope 1适用范围

This document shall be applied to 0.95~5.0 TFT-LCD Panel.

本文件适用于0.95~5.0 TFT-LCD Panel.

2.Inspection and Environment onditions/检查条件与环境

2. 1 Inspection Conditions 检查条件:

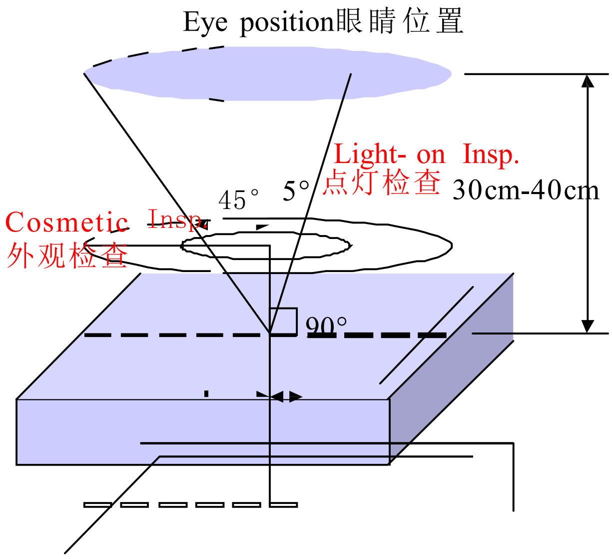
(1) Inspection Distance检测距离: 35 cm±5cm

(2) Each picture /每个画面： 2~3 secs/秒， Cosmetic Inspection/外观10~12 secs/秒

(3) View Angle观看角度:

Light-on Inspection Angle点灯检验角度 ： ±45°

Cosmetic Inspection Angle外观检验角度 ： ±45°



(Perpendicular to LCD panel surface垂直于液晶显示表面)

2.2 Environment Conditions环境条件:

Ambient Temperature 温度		25℃±5℃
Ambient Humidity 湿度		55±5%RH
Ambient Illumination 亮度	Cosmetic Inspection 外观检验	800-1000 Lux
	Functional Inspection 点灯检验	200~300Lux

2.3 Sampling Conditions 抽样条件:

(1) Lot Size： Quantity of shipment lot per model/.

批量：单次运送单一机型数量

(2) Sampling Method ：
抽样方法：

Sampling Plan 抽样计划		GB2828/2003
		Normal Inspection, Single Sampling 正常检验、单次抽样
		Geneal II Inspection 普通二级
AQL	Major Defect 主要缺点	0.25
	Minor Defect 次要缺点	0.65

(3) The classification of Major(MA) and Minor(MI) defects is shown as 3. Inspection Criteria.
主缺(MA)及次缺(MI)定义于”3.检查标准”

3.Terms and Definitions/术语和定义

3.1 Classification of defects缺陷的分类:

Major defects: A major defect is a defect that is likely to result in failure, or to reduce materially the usability of the product for its intended purpose.

主要缺陷：会导致产品功能失效或减少产品可用性的缺陷。

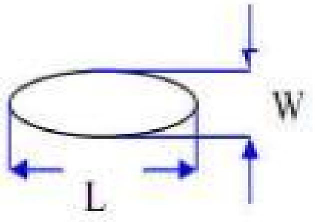
Minor defects: A minor defect either is a defect that is not likely to reduce materially the usability of the product for its intended purpose, or is a departure from an established having little bearing on the effective use or operation of the product.

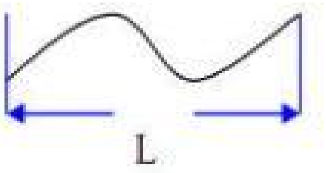
次要缺陷：不会导致产品功能失效，不会减少产品的有效使用和操作。

3.2 Extraneous substances that can be wiped out ,like Finger point,Particles are not cnsidered as a defect . 可以被擦拭干净的表面物质不视为缺陷 (如手指印，尘粒) 。

3.3 Defects on the Black Matraix(outside ofActive Area) are not considered as a defect . BM 区域 (AA 区以外) 的缺陷不视为缺陷。

3.4 Size of circular defect,is defined by diameter”D” 。The defect average diameter D=1/2(W+L) 圆形缺陷的大小是由直径 D 定义的。缺陷的平均直径 D=1/2(W+L)





3.5 When defect size L≥2W,the defect count as liner type defect.Size of linear defect is defined by length(L) and the maximum width(W).

当缺陷尺寸 L≥2W 时，被视为线状缺陷。线状缺陷是由长度 (L) 和最大宽度 (W) 定义的。 3.6 3.6 Mura criteria :judged by ND filter6%,and can’t be seen under at ND filter 6% .

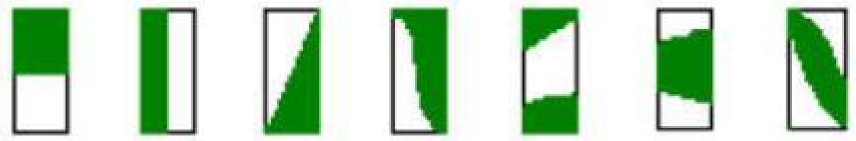
3.6 MURA 判断标准：使用 ND6%判定，且透过 ND6% ， 遮住不可见.

3.7 Dot defect is defind as the defective area of the dot is larger than 50% of the dot area and is visible through 6% ND filter

DOT 定义为点缺陷面积大于 50% DOT 面积, 且透过 ND6%遮住是可见的.

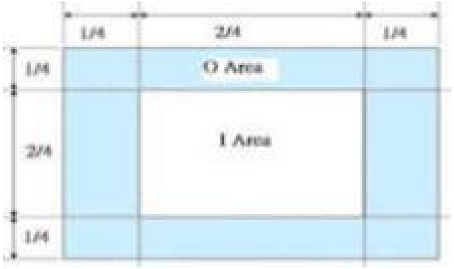
The drawing of 1/2 area sub-pixel definition: The 1/2 area sub-pixel can be defined as below one or more of specific shapes

1/2 面积的子像素定义绘图：1 / 2 面积的子像素可以定义为如下一个或多个特定形状图：



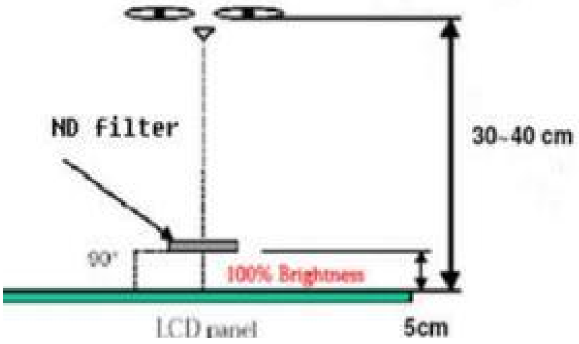
3.8 A dot defect that is smaller than the defined dot defect will be treated as small bright dot. 细碎亮点：小于“DOT 定义”的点缺陷视为细碎亮点。

I 区与 O 区比例：1：2：1



3.9 Inspection method of ND Filter - holding ND filter in front of the panel around 5cm and examine the panel from 35±5 cm in the front view for 2~3 second.

ND 卡的检查方法：在面板上方大约 5CM 处握住 ND 卡，眼睛距离面板 30-40CM ，通过 2~3 秒观察。



4. Inspection Criteria 检验标准

4.1 Appearance Inspection specification 外观检查规格:

Judge area **区域**	**Judge item** **项目**	**Specification inspection** **检查规格**	**Judge criterion**	
			Major	**Minor**
Silicone 硅胶	Silicone spread 硅胶涂布	The height can’t over C/F， color filter， or gomu 高度不能过超 C/F		MI
	Silicone residue 硅胶残余	Can’t cover polarizer，FPC …etc. 不能覆盖 POL，FPC 等		MI
LCD 玻璃	Wire(on Array) 线路	No damage 不能损伤	MA	
	Edge 边缘	No extended crack 不可有延伸性裂纹	MA	
PCBA Connector FPC/FFC	Appearance 外观	Scratch or damage result in copper expose is not allowed 划伤或损伤不允许导致出现露铜		MI
	Component 零件	No damage 不能损伤	MA	
	Connection status 连接状况	Need correct connection 需要正确连接	MA	
	Broken 破裂	Not allowable 不允许	MA	
	Folding sign 对位记号折叠	Not allowable 不允许	MA	
POL 偏光片	Scract on the polarizer 偏光片划伤	1.W≤0.05mm；L≤5mm，Ignore（忽略）		MI
		2.0.05mm<W≦0.10mm ; L≤5mm ; N≤3 ; DS≥10mm		
		3.0. 10mm＜W；5mm＜ L，Not allowable不允许		

Judge area 区域	Judge item 项目	Specification inspection 检查规格	Judge criterion	
			Major	Minor
POL 偏光片	Dent on the polarizer 偏光片凹痕	1.D＜0. 15mm，Ignore（忽略）		MI
		2.0.15mm＜D≤0.30mm；N≤3；DS≥10mm		
		3.0.30mm＜D，Not allowable不允许		
	POL Linear bubble 线状气泡	1.W≤0.05mm；L≤5mm，Ignore（忽略）		MI
		2.0.05mm<W≦0.10mm ; L≤5mm ; N≤3 ; DS≥10mm		
		3.0. 10mm＜W；5mm＜ L，Not allowable不允许		
	POL dot bubble 点状气泡	1.D＜0. 15mm，Ignore（忽略）		MI
		2.0.15mm＜D≤0.30mm；N≤3；DS≥10mm		
		3.0.30mm＜D，Not allowable不允许		
	POL edge bubble 片边缘气泡	1. The display area is 1/2BM outside，Not allowable 显示区往外 1/2BM 区域内，不允许 2. The display area is outside the outer 1/2BM area，Not allowable 显示区往外1/2BM区域以外，不管控		MI

Judge area **区域**	**Judge item** **项目**	**Specification inspection** **检查规格**	**Judge criterion**	
			Major	**Minor**
TP&CG	Foreign Material in spot shape 点状异物	1.D≤0.15mm；Ignored（忽略） 2.0.15mm＜D≤0.30mm；N≤3；DS≥10mm 3.D＞0.30mm；Not allowable不允许		MI
	Fisheye/bubbles 鱼眼/气泡	1.D≤0.15mm；Ignored（忽略） 2.0.15mm＜D≤0.30mm；N≤3；DS≥10mm 3.D＞0.30mm；Not allowable不允许		MI
	Scratches on the surface 表面划伤	1.W≤0.05mm；Ignored（忽略） 2.0.05mm<W≤0.10mm，L≤5mm；N≤3；DS≥10mm 3.W＞0.10mm，L＞5mm；Not allowable不允许		MI
	Collapse corner、Crash edge 崩角、崩边	Product front:/产品正面： collapse corners, collapsed edges are not allowed 崩角、崩边不允许； Product back/产品背面： X≤ 0.5 , Y≤0.5，Z≤1/2T；N≤2；DS≥10mm	MA	
	Printed fonts/LOGO 丝印/LOGO	Printed fonts/LOGO clarity、complete、content right 字体/LOGO丝印清晰、完整、内容正确		MI
	Broken 破损	Not allowable不允许	MA	
	Dirty surfaces 表面脏污	Dirt cannot be wiped，Not allowable 不可擦拭的脏污，不允许		MI
	IR hole IR孔	Black spots/黑点： W ≤0.15mm，N≤2，Not visible against a black background/黑色背景下不可见		MI
		IR hole Scratches： 1.W＜0.03mm，Ignored（忽略） （Dense points Not allowable 不允许密集）； 2.0.03mm＜W≤0.08mm；L≤2mm；N≤2； 3.W＞0.08mm，L＞2mm，Not allowable 不允许		MI

4.2 Electrical Inspection specification电性检查规格:

Item **项目**	**Judgment Criteria** **判定标准**	**Judge criterion**	
		Major	**Minor**
LCD Bright /Dark dot 玻璃亮点/暗点	1.D≦0. 15mm， Ignored（忽略）， Not dense（不可密集） 2.0.15mm<D≦0.30mm； N≦3； DS≥10mm 3.D＞0.30mm， Not allowed/不允许		MI
Mura	Invisible through 6% ND filter，200~300Lux 透过ND6% 遮住， 目测不可见即为OK， 200~300Lux		MI
Small bright dot 细碎亮点	Not allowed if it can be observed through ND Filter6% 透过ND6%目测看得见，不允许		MI
ZBD Rate 玻璃亮点比率	90:10		MI
Light Leakage 漏光	Invisible through 6% ND filter，OK 透过ND6%遮住目测不可见即为OK If necessary,set up set up Limit Sample. 如果有必要，可制订限度样品		MI
Bubble in Cell (LC Bubble/Actice Area) CELL气泡 (AA区LCD气泡)	Eyes should not find it . 目视观察不可见，视为 OK	MA	

Item **项目**	**Judgment Criteria** **判定标准**	**Judge criterion**	
		Major	**Minor**
Foreign Material in spot shape 点状异物	1.D≦0.15mm， Ignored（忽略） 2.0.15mm<D≦0.30mm； N≦3； DS≧10mm 3.D＞0.30mm， Not allowable/不允许		MI
Foreign Material in line or spiral shape 线状异物	1.W≦0.05mm， Ignored（忽略） 2. L≤5mm； 0.05mm<W≦0.10mm ； N≦3 3.W＞0.10mm； L＞5mm， Not allowable/不允许		MI
White dot in back-light 白点	1.D≦0. 15mm，Ignored（忽略） 2.0.15mm<D≦0.30mm； N≦3； DS≥10mm 3.D＞0.30mm， Not allowed/不允许		MI
TP no touch 无触摸	Not allowable 不允许	MA	
Abnormal Disply 显示异常	Not Allowed 不允许	MA	
NO display 无显示	Not Allowed 不允许	MA	
Line Defect 缺线	Not Allowed 不允许	MA	
Angle of view error 视角错误	Not Allowed 不允许	MA	
Tect crostalk 不消失的残影	Not Allowed 不允许	MA	